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09/769,953	01/25/2001	Sompong P. Olarig	COMP:0195	5912

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EXAMINER	
LE, DIEU MINH T	

ART UNIT	PAPER NUMBER
2114	8

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/769,953	Applicant(s) OLARIG, SOMPONG P.	
	Examiner Dieu-Minh Le	Art Unit 2184	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 January 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 7 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Part III DETAILED ACTION

Specification

1. Claims 1-50 are presented for examination.

Double Patenting Rejections

2. Claims 1-50 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-8 of U.S. patent 6,018,810. Although the conflicting claims are not identical, they are not patentably distinct from each other because the claimed subject matter contains obvious modifications to previous claims 1-8 of U.S. patent 6,018,810.

As to claims 1, 27 and 40, these claims include limitations of: fault-tolerant interconnect system, first type bus and second type bus having first bus portion and second bus portion, device interface configured to detect errors in a transaction wherein if a first error is detected on the firs bus portion, the transaction is performed over the second bus portion, and if a second error is detected on the second bus portion, then the transaction is performed over the first bus portion; which already included in claims 1-8 of U.S. patent 6,018,810. It is well settled that the omission of an element and its function

[i.e., a processor or an initiator] is an obvious expedient if the remaining elements perform the same function as before. In re Karlson, 136, USPQ 184 (CCPA 1963). Also note Ex parte Rainu, 168 USPQ 375 (Bd. App. 1969). Therefore, omitting various elements from the previous claimed subject matter would have been obvious to one of ordinary skill in the art in this case since the remaining elements do in fact perform the same functions as before. Elimination/Changing of an element or its function will not serve as a basis for patentability.

4. The obviousness-type double patenting rejection is a judicially established doctrine based upon public policy and is primarily intended to prevent prolongation of the patent term by prohibiting claims in a second patent not patentably distinct from claims in a first patent. *In re Vogel*, 164 USPQ 619 (CCPA 1970). A timely filed terminal disclaimer in compliance with 37 C.F.R. § 1.321(b) would overcome an actual or provisional rejection on this ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 C.F.R. § 1.78(d).

Claim Objections

3. The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

Misnumbered claim 37, claims 38 - 50 need to be renumbered 37 - 49. Correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-8, 13-30, 35-42, and 44-50 are rejected under 35 U.S.C. § 102(b) as being anticipated by Garbus et al. (US Patent 5,884,027 hereafter referred to as Garbus).

As per claims 1, 6-8:

Garbus explicitly teaches:

- a computer system [fig.2]

comprising:

- a host bus [abstract];

- an input/output [I/O] fault-tolerant interconnect system [col.1, line 12, fig.2]; and

- a core logic chipset comprising a configurable bridge interface connectable between the host bus and the I/O fault-tolerant interconnect system [col.2, lines 15-20];

- an I/O bus selectively comprising one of a first type bus and a second type bus, the I/O bus comprising a first bus portion and a second bus portion [fig.2, #17, the primary PCI bus is the first portion and #19, the secondary PCI bus is the second portion];

- a device interface connectable to the I/O bus, wherein the first device interface is configured to detect errors in a transaction received by the device interface [col.6, lines 51-57; col.7, lines 17-21] wherein,

- if a firs error is detected on the first bus portion, the transaction is performed over the second bus portion [col. 16, table 4b];

- if a second error is detected on the second bus portion, then the transaction is performed over the first bus portion [col. 17, table 4c].

As per claim 2:

Garbus explicitly teaches:

- if both the first and second errors are detected, then the transaction is terminated [col. 17, table 4c].

As per claim 3:

Garbus explicitly teaches:

- the first error and the second error comprise parity errors [col. 17, table 4c].

As per claims 4-5:

Garbus explicitly teaches:

-the peripheral component interconnect bus comprises a PCI-X bus[abstract, fig.2].

As per claim 13:

Garbus explicitly teaches:

-the I/O bus comprises a 64-bit bus, and wherein the first bus portion is a first 32-bit bus and the second bus

portion is a second 32-bit bus [fig.4, col.10, lines 43-46].

As per claim 14:

Garbus explicitly teaches:

- the configurable bridge interface is configured in response to receipt of a configuration signal [col.2, lines 23-29].

As per claim 15:

Garbus explicitly teaches:

- the configuration signal is generated by a hardwired jumper circuit [fig.5, col. 4, lines 14-22].

As per claims 16-18:

Garbus explicitly teaches:

- the core logic chipset comprises at least one integrated circuit wherein the at least one integrated circuit having at least one application specific integrated circuit, one programmable logic array integrated circuit [col. 2, lines 9-18, col.56, lines 30-33].

As per claims 19-21:

Garbus explicitly teaches:

- the host bus and the I/O bus are disposed on a substrate wherein the substrate is a printed circuit board [col. 2, lines 9-18].

As per claim 22:

Garbus explicitly teaches:

- the configurable bridge interface is configured for either the first type bus or the second type by software control of the core logic chipset [col.3, lines 29-35].

As per claim 23:

Garbus explicitly teaches:

- the configurable bridge interface is configured for either the first type bus or the second type bus when either a first type device or a second type device, respectively, is detected on the I/O bus [fig.10, col.55, lines 15-50].

As per claim 24:

Garbus explicitly teaches:

- the first type device comprises an accelerated graphics port device, and the second type device comprises a

peripheral component interconnect device [col.56, lines 41-46].

As per claim 25:

Garbus explicitly teaches:

- the configurable bridge interface is configured during power on self test of the computer system [col.24, lines 66 to col.25, line 2].

As per claim 26:

Garbus explicitly teaches:

- the configurable bridge interface is configured during configuration of the computer system [fig.2].

This is clearly shown that Garbus's architecture for an I/O processor that integrates a PCI to PCI bridge system does illustrate, demonstrate, and teach capabilities corresponded to Applicant's invention.

As per claims 27-30, 35-36, 38-39:

These claims are the same as per claims 1-8, 13-26. Therefore, these claims are also rejected under the same rationale applied against claims 1-8, 13-26.

As per claims 40-50:

Due to the similarity of claims 40-50 to claims 1-8, 13-26 except for a method of configuring a core logic chipset for connecting between a host bus and a fault-tolerant input/output bus instead a system one; therefore, these claims are also rejected under the same rationale applied against claims 1-8, 13-26.

Allowable Subject Matter

5. Claims 9-12, 31-34, and 43 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. However, these claims are still subject under double patenting rejection indicated in paragraph above.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

7. A shortened statutory period for response to this action is set to expired THREE (3) months, ZERO days from the date of this

letter. Failure to respond within the period for response will cause the application to be abandoned. 35 U.S.C. 133.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dieu-Minh Le whose telephone number is (703) 305-9408. The examiner can normally be reached on Monday-Thursday from 6:30 AM to 4:00 PM. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel, can be reached on (703)305-9713. The fax phone number for this Group is (703)746-7240.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 746-7239, (for formal communications intended for entry)

Or:

(703) 746-7240 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

DIEU-MINH THAI LE
PRIMARY EXAMINER
ART UNIT 2114

DML
12/12/03